

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Frederic Reblewski

Application No.: 10/043,964

Filed: Jan. 10, 2002

For: CROSSBAR DEVICE WITH
REDUCED PARASITIC
CAPACITIVE LOADING AND
USAGE OF CROSSBAR DEVICES
IN RECONFIGURABLE CIRCUITS

Examiner: Sun J Lin

Art Unit: 2825

Confirmation No.: 6410

Customer No.: 25943

Mail Stop Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.323

Dear Commissioner:

Upon review of the above-referenced Letters Patent, Applicant noted errors that are the mistake of the U.S. Patent and Trademark Office.

Please correct the following:

at col. 5, line 24, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 5, line 44, "raise a voltage raised by" should read --raise a voltage by--

at col. 5, line 53, "wherein each the" should read --wherein each of the--

at col. 5, line 54, "pass transistors coupled" should read --pass transistor coupled--

at col. 5, line 58, “transistor; where” should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 5, line 65, “wherein each the” should read --wherein each of the--

at col. 6, line 3, “transistor; where” should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 6, line 7, “coupled a pass” should read --coupled to a pass--

at col. 6, line 13, “reconfigurable logic circuit” should read --reconfigurable circuit--

at col. 6, line 35, “wherein each the” should read --wherein each of the--

at col. 6, line 40, “transistor; where” should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 6, line 53, “transistor; where” should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 8, line 2, “some know logic” should read --some known logic--

Applicant believes no fee is required for these corrections. It is respectfully requested that a Certificate of Correction be issued.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: August 27, 2009

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 6,874,136
APPLICATION NO.: 10/043,964
ISSUE DATE : 03-29-2005
INVENTOR(S) : Frederic Reblewski

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 5, line 24, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--.

Column 5, line 44, "raise a voltage raised by" should read --raise a voltage by--.

Column 5, line 53, "wherein each the" should read --wherein each of the--.

Column 5, line 54, "pass transistors coupled" should read --pass transistor coupled--.

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Column 8, line 2, "some know logic" should read --some known logic--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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